Emerging Technologies in Random Access Memories

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Abstract- Memories based on charge storage principle are used since many decades. The greater speed and higher density of memory chips are now achieved at lower costs. However, speed and size are gradually approaching the physical limits. Newer memory concepts are therefore being explored. This paper presents a discussion on different random access memories based on new concepts. An overview of emerging technologies, probable future trends and challenges are described.

Keywords- Random Access Memory, Capacitorless DRAM, ZRAM, PCRAM, ReRAM, MRAM, FeRAM

I. INTRODUCTION

The embedded memory takes more than two third of the chip area in many of today’s processors [1]. This trend is expected to increase in future. Scalability, high speed of operation, low power consumption, low operating voltages, long retention time and high endurance are essential features for any type of memory cell. Memory technologies based on charge storage principle have been developed to achieve these requirements.

However, memories based on charge storage principle are approaching their physical limits. Nano-scale processing has complexity and thus high manufacturing cost. New cell structures for RAM are therefore, researched for scale size below 20 nm. Many new memory concepts are thus being researched and presented to overcome the various limitations. This paper gives a review the emerging technologies. It also describes the advantages and their limitations for future use.

II. CAPACITORLESS DRAM

SRAM is the fastest memory. It needs 4-6 transistors for one memory cell. Therefore, it is more suitable for high performing memories with limited size requirement, for example, L1 cache.

Dynamic random access memory (DRAM) is not as fast but requires smaller cell area. This makes it an attractive option for embedded memories of large size, for example, L2 cache.

![Fig. 1: Schematic of DRAM (a) With capacitor - 1T1C cell (b) Capacitorless – 1T0C cell](image-url)
A basic DRAM cell consists of one access transistor and a storage capacitor. The capacitance of the storage capacitor is not scalable in the cell. The capacitor requires complex geometries [2], [3]. Therefore the yield is poor. There is thus additional cost. Another requirement for switching transistor is that it must maintain a drive current of about 25 µA with an extremely low leakage current of about 1 fA [4].

Recently, alternative capacitorless DRAM concepts have been proposed in order to simplify the manufacturing processes. The cells possessing floating-body and floating-body/gate (ZRAM) have been proposed and investigated [5] recently. Figure 1 shows schematic for DRAM 1T1C cell as well as 1T0C cell.

A ZRAM cell consists of only one transistor which is fabricated using SOI technology. It is five times denser than SRAM cell and two-three times denser than DRAM cell [6]. ZRAM memories have therefore, potential of widespread use in commercial embedded memory applications in near future. The gated diode with enhanced gate control is also called tunneling field-effect transistor (TFET). A floating junction gate memory cell using TFET as write transistor has been proposed for ultradense DRAM applications [7].

FinFET present symmetric-gate stack material. FinFETs are considered for advanced CMOS platforms to overcome major drawbacks such as short channel effects and process variations [8]. Independent double-gate (IDG) thin film transistors can be considered potential capacitorless DRAM when two electrically independent gates are available. The first gate manages the front transistor and the second gate allows charge accumulation through body potential. The use of vertical gate-all around transistors extends the capacitorless DRAM roadmap to future generations [9].

DRAM structures using III-V wide energy-band gap compound-semiconductors are also being considered. These semiconductors have enhanced properties. They will have lower leakage currents and therefore, may show better retention time [10].

III. PHASE CHANGE RAM

PCRAM is the most mature of the new emerging memory technologies. PCRAM cells work by switching a fragment of chalcogenide glass between amorphous and crystalline states, which have different resistivities. Ge2Sb2Te5 is one of the commonly used materials [11]. Phase changes are brought by Joule heating from electrical current. Schematic diagram of PCRAM is shown in figure 2.

![Schematic of a PCRAM](image-url)
Emerging Technologies in Random Access Memories

Amorphous state with high resistance is programmed by melting and quenching. Crystalline state with low-resistance is programmed by annealing the glass. PCRAM does not have high speed as that of DRAM. It also lacks high storage density as compared to other available memory e.g. Flash. But it has higher endurance than NAND Flash. It may have applications in some niche areas viz. aerospace. When other memories would fail under radiation, it keeps working.

IV. RESISTIVE RAM

ReRAM works by forming or breaking minuscule conductive pathways through normally insulating materials. It changes the resistance of storage node by applying current or voltage bias. Many metal oxides show such characteristics. Switching mechanisms are expected to be ionic migration and redox reactions. Low programming power, fast switching speed and scalability beyond 10 nm have been demonstrated by various researchers [12], [13]. It has good but lower endurance presently when compared with MRAM. The cell material gets fatigued over time. Manufacturing and material difficulties restrict its availability and use. Also, it is still in early research stage.

V. MAGNETORESISTIVE RAM

MRAM replaces the capacitor of a DRAM cell with a pair of magnets. One magnet has a fixed polarity while other can be flipped. The memory cell is programmed by flipping the movable magnet. It is read by sensing the resultant change in resistance. The primary building block of MRAM is a single access transistor in series with a single magnetic tunnel junction (MTJ) resistor (1T1R). Fig. 3 shows the schematic of the three layer MTJ in state 1 and in state 0.

Spin transfer torque MRAM (STT-MRAM) does not require an external magnetic field. It consists of thin insulating tunneling barrier e.g. MgO, between two Ferromagnetic layers [15]. The resistance of the memory cell changes depending on the relative direction of magnetization of two ferromagnetic layers. It is expected to have almost infinite endurance, long retention, high bandwidth, low read/write latency. Scalability seems to be an issue. The cost structure of MRAM is a hindrance in its wide spread use.

![Fig. 3: Schematic of the three-layer MTJ in (a) state ‘1’: Large resistance and (b) state ‘0’: Low resistance state](image-url)
VI. FERROELECTRIC MEMORY

Ferroelectric RAM (FeRAM) store data by modulating the polarization of a ferroelectric capacitor. The charge is sensed by applying appropriate voltage. Basic unit memory cell consists of an access transistor and a ferroelectric capacitor (1T1C). Compared to other technologies, it has lower power consumption and high speed write operation. Its wide use may be restricted by its wear out mechanism which limits its endurance. Similar to DRAM, its read process is destructive. Therefore the data need to be refreshed after the read cycle. This makes it not so desirable for low-power applications. Cost structure of FeRAM is not very competitive and cell sizes are larger than 30F² (F~ Feature size) [16].

Table 1: Comparison of RAM Technologies

<table>
<thead>
<tr>
<th>Memory type</th>
<th>Capacitorless DRAM</th>
<th>PCRAM</th>
<th>MRAM</th>
<th>FeRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell</td>
<td>Floating gate</td>
<td>Phase Change</td>
<td>Magnetoresistive</td>
<td>Ferroelectric</td>
</tr>
<tr>
<td>Structure</td>
<td>1T0C</td>
<td>1T1R</td>
<td>1T1MTJ</td>
<td>1T1C</td>
</tr>
<tr>
<td>Application</td>
<td>Main Memory</td>
<td>Storage</td>
<td>Storage</td>
<td>Storage</td>
</tr>
<tr>
<td>Feature size (F)</td>
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<td>6-10F²</td>
<td>6-10F²</td>
<td>6-10F²</td>
</tr>
<tr>
<td>Endurance</td>
<td>Infinite</td>
<td>&gt;10¹²</td>
<td>&gt;10¹⁵</td>
<td>&gt;10⁸</td>
</tr>
<tr>
<td>Read/Write speed</td>
<td>1 ns/1 ns</td>
<td>20ns/50ns</td>
<td>10ns/10ns</td>
<td>10ns/10ns</td>
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<tr>
<td>Cost efficiency</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
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<td>Reliability</td>
<td>Yes</td>
<td>Yes</td>
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</tbody>
</table>

VII. CONCLUSIONS

Existing memories are facing various issues in terms of scalability, power consumption, endurance, retention and manufacturability. Paper gives a review of various emerging memory technologies that are being researched. Table 1 shows the comparison of various RAM Technologies. It is hoped that these memories will overcome the present challenges. Long term scalability and endurance along with lower power use will ultimately decide their applications in future devices and circuits.

REFERENCES

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